

Nicola Vincenti's Curriculum vitæ

(Updated to 15th Oct 2011)

PERSONAL DATA:

Name	Nicola	Home telephone number	+39 050/9662935
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PRESENT POSITION

From 23rd February 2011 – Test Engineer at Intel, Swindon – United Kingdom

EDUCATION

Course attendance of *J750 Mixed Signal Option programming, J750 Converter Test Option programming*, located in Teradyne, Rousset, May 2007.

Master in Microelectronic design (University of Padova), May 2007. Result: positive with merit.

Degree in Electronic Engineering obtained in Pisa, December 2002. (Old ordination, 5 years course). Result 108 out of 110.

Scientific diploma, July 1994. Result: 54 out of 60.

Registration to the professional engineer album on year 2003.

Certificate of English language knowledge FCE on year 2001

Diploma of music Teoria and Solfeggio at Conservatorio of La Spezia, year 2000-2001.

WORKING EXPERIENCES

Da Febbraio 2011

- Test Engineer in Intel, Swindon UK.
Implementation of verification test programs at package and wafer level on Teradyne UltraFlex test system.

From January 2008 to November 2009

- Continuation of the same role in Navacchio (Pisa) as Sensor Dynamics AG employee

From December 2006 to December 2007

- Employed in Sensor Dynamics AG, Navacchio, PI - Italy – Graz, Austria
- Location of work: Graz, Austria

Functional and parametric verification of electrical and inerzial parameters, test bench analysis, implementation of test program suited to cover and screen production and validation defects. Programming scripts for translation of inter-instrumental pattern formatted according to industrial standards in electronic. Statistical analisys of reliability and producibility respect to production ramp up. Strategies for team work.

Experiences in implementing test programs for validation of digital circuits and mixed signal circuits (micro-dsp-mixed signal)

From June 2006 to December 2006

- Stage at Istituto Nazionale di Fisica Nucleare.
- Location: Ferrara

Design and simulation of telecommunication algorithms for satellite systems (6 months introduction to the project).

From August 2003 to August 2005

- Employment in Microtest srl, Altopascio, LU
- Location: ST-Microelectronics Agrate – Milano. Mission abroad (Malta) for transfer of production tecnology.

External consultant for board and probe card design, technology instruments for validation and production of automated circuit production systems. Implementation of validation programs (more than one phase) of circuits verification and screening. Product specification analysis and verification. Exchange of information with customers and suppliers relative to technical details on design issues and electronic components issues (in italian and english language).

In particular paralell programming of J750 test system for verification and screening of production of digital circuits (ST10 micro-controller)

Maggio 2003 – Agosto 2003

- Stage in Microtest srl, Altopascio, LU
- Location: Altopascio, LU

Usage of programming informative technics and electronic knowledge for design of boards for microelectronic circuit production.

EXPERTISE

Optimal knowledge of hardware description language: VHDL and Verilog.

Experience on FPGA Altera and Xilinx usage for design process and relative tools for simulation.

Implementation of complete programs for the verification of technical specification of microelectronic circuits.

Experience on design and test of digital circuits and mixed signal circuits in CMOS technology.

Programming in C/C++ and Java, both for microcontroller and PC.

Experience on design of layers for circuits implementation.

Programming scripts in Python.

Practice in the usage of electronic instrumentation: oscilloscope, multimeter, wave signal generator.

NON PROFESSIONAL QUALIFICATIONS

Microsoft Office software knowledge

HTML, Javascript and ASP knowledge

PERSONAL HOBBIES AND ATTITUDES

classical music enjoy, sports (swimming and jogging), card table games

With the introduction of this notice I acknowledge the treatment of my data according to italian law n. 196/2003.

Pisa, 15th October 2011

Sign: _____